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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,040	LIN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 and 16-24 are pending in the present application.

Drawings

The drawings were received on 6/28/06. These drawings are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-14 and 16-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Kirk U.S. Patent No. 6,968,485 in view of Smith et al. U.S. Patent No. 6,944,692.

As per claims 1, and 13, Van Kirk teaches the claimed method for testing signals of integrated circuits (ICs), comprising the steps of: successively driving, by a first IC chip, a plurality of test patterns one at a time; receiving, at a second IC chip, and latching in the test patterns on by one; determining, whether a currently latched test pattern is correct; if at least an error bit occurs in the currently latched test pattern, the second IC chip indicating that there exists noise interference in a signal trace corresponding to the error bit; and repeating the above steps until the first IC chip finishes driving the test patterns (Abstract, Figure 1, 155). And also teaches if the currently latched test pattern is incorrect, adjusting a reference voltage level in accordance with the type of the corresponding test pattern to change an input threshold of the second IC chip (column 1 line 39-40, column 2 line 12-15, column 2 line 55-60, column 3 line 40-45). Not disclosed by Van Kirk is the use of a second chip to identify an error.

However, in an analogous art, Smith et al. teach a second chip coupled as a receiver, which determines if the correct data is received (column 4 line 66 through column 5 line 9, column 11 lines 26-56). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used

the second chip as a receiver in the method as described by Van Kirk, One would be motivated to make this combination as disclosed by Smith et al. in order to properly set timing and voltages on a circuit board thus ensuring proper operation of a system (column 1 lines 24-39).

As per claims 2 and 14, Van Kirk teaches the test patterns are at least divided into three types including a ground bounce type, a power bounce type and a heavy load type (column 11 line 32 and column 20 line 50-60).

As per claim 3, Van Kirk teaches the step of: if the currently latched test pattern is incorrect, the second IC chip adjusting a reference voltage level in accordance with the type of the corresponding test pattern to change an input threshold of the second IC chip (column 1 line 39-40, column 2 line 12-15, column 2 line 55-60, column 3 line 40-45).

As per claims 4 and 16, Van Kirk teaches the reference voltage level is decreased to lower the input threshold of the second IC chip if the corresponding test pattern belongs to the power bounce type (Figure 15, column 4 line 60, column 12 line 36-45, column 14 line 63, column 13 line 1-20).

As per claims 5–7 and 17-19, Van Kirk teaches the techniques of testing reference voltages as noted in claims 2, 3, and 4. (Figure 15, column 4 line 60, column 12 line 36-45, column 14 line 63, column 13 line 1-20).

As per claims 8 and 20, Van Kirk teaches the step of: adjusting a driving capability of a pin relative to the error bit for the first IC chip to change the pin's output timing (Abstract, Figure 1, 155).

As per claims 9 and 21, Van Kirk teaches the driving capability of the pin relative to the error bit is increased to advance the pin's output timing for the first IC chip (column 3 line 40-45).

As per claims 10 and 22, Van Kirk teaches the driving capability of the pin relative to the error bit is decreased to delay the pin's output timing for the first IC chip (column 4 line 60, column 12 line 36-45).

As per claims 11 and 23, Van Kirk teaches the method of claim 8 wherein the output timing is changed in a unit of 150 ps at a time when adjusting the pin's driving capability for the first IC chip (column 3 line 10-20).

As per claim 12 and 24, Van Kirk teaches the output timing is adjusted by changing an internal register setting of the first IC chip (Figures 2A and 2B).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138